**Project Title  
Digital Counter Circuit**

**Group Members**

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### **1. Executive Summary**

**Overview:**This project involves the design and simulation of a basic digital counter using a 555 Timer and two 4026 ICs. The aim is to visualize how digital pulses generated by a timer can control a dual-digit numerical display, counting from 00 to 99. The project reflects structured and modular logic behavior, analogous to OOP concepts.

**Key Findings:**The team successfully implemented a real-time counter simulation using Proteus, showcasing how pulse-driven logic circuits can simulate counting operations using standard digital ICs.

### **2. Introduction**

**Background:**Digital electronics serve as the basis of modern embedded systems and computing devices. Understanding counters is fundamental to mastering hardware logic. This project introduces core digital components and highlights how timing pulses translate into countable digital outputs.

**Project Objectives:**

* Design and simulate a 555 Timer-based pulse generator.
* Use two 4026 ICs to count pulses and display output on 7-segment displays.
* Demonstrate pulse-to-count translation in a real-time simulated circuit.

### **3. Project Description**

**Scope:**

**Included:**

* 555 Timer in astable mode
* Two 4026 Decade Counter ICs
* Two 7-segment displays
* Proteus simulation and visualization

**Excluded:**

* No microcontroller programming
* No sensor integration or external input systems

**Technical Overview:**

* **Software:** Proteus Design Suite
* **Hardware Components:**
  + 555 Timer IC
  + 4026 ICs
  + Common cathode 7-segment displays
  + Basic passive components (resistors, capacitors)

### **4. Methodology**

**Approach:** An iterative workflow was followed: design → simulate → test. The project was divided into phases, enabling collaborative development and frequent validations.

**Roles and Responsibilities:**

* **Muhammad Baqar:** Timer circuit design and pulse generation simulation
* **Kashif Mehmood:** Counter IC integration and display wiring
* **Joint effort:** Documentation, presentation, and final testing

### **5. Project Implementation**

**Design and Structure:**

* The 555 Timer was configured in astable mode to produce a continuous square wave.
* The output pulse was connected to two cascaded 4026 ICs, each driving a single 7-segment display.
* The first IC handles unit counts (0–9), the second handles tens (10–99).

**Functionalities Developed:**

* Automated pulse generation.
* Real-time count increment with display.
* Modular IC connections allowing scalable extension.

**Challenges Faced:**

* Achieving stable timing in simulation without signal bounce.
* Synchronizing the second counter (tens digit) with the overflow from the first.
* Resolved using careful timing calibration and logic probing in Proteus.

### **6. Results**

**Project Outcomes:**

* A fully functional simulation of a dual-digit digital counter.
* Demonstrated understanding of pulse logic, IC interconnections, and display control.

**Testing and Validation:**

* The circuit was tested under varying frequency settings.
* Edge detection validated through waveform analysis tools in Proteus.

### **7. Conclusion**

**Summary of Findings:** The digital counter circuit successfully fulfilled its intended objectives, offering a strong learning experience in both simulation and digital logic design. It emphasized structured logic behavior similar to OOP modularity.

**Final Remarks:** This project deepened our understanding of hardware-based logic systems and provided hands-on experience in digital circuit design without the need for microcontrollers or coding.